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CX20501

Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)
Data Sheet

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Contents

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Key Features

- Four independent CDRs, each running between 65 Mbps and 3.2 Gbps
- Jitter generation 7 mUI, Jitter Tolerance 0.6 UI typical
- Typical Total Power Consumption as low as 900 mW with all channels running
- Per channel bypass mode for unsupported data rates
- Per channel power-down mode for unused channels

Applications

- SONET OC-1, OC-3, OC-12, OC-48 systems and modules
- InfiniBand systems and modules
- Digital Video Applications (SDI and HDI)
- Fibre Channel (1x, 2x, 10x) systems
- Gigabit Ethernet systems
- 10GBASE-LX4 XAUI systems & modules
- ESCON, FDDI, NTSC/PAL systems and modules
- Backplane reach extension

Product Description

The CX20501 is a quad Clock and Data Recovery (CDR) circuit designed for +3.3 or +2.5 V low power operation. As a multi-rate device, it can support data rates from 65 Mbps to 3.2 Gbps. Because each CDR operates independently, each can lock to a common frequency or to a separate frequency to support diverse applications without an external frequency reference. A quasi-limiting amplifier is used to improve the input sensitivity of the device. To save power, the individual output clocks and/or CDRs can be powered down and the output drive level is also selectable. The high-speed I/O is differential Positive Current Mode Logic (PCML) with an on-chip 50 Ω to Vdd (single-ended) input termination/output backmatch. The I/O can be used either differentially or single-ended. A serial interface (+3.3 V/+2.5 V CMOS) is used to fine-tune the frequency acquisition characteristics and the operating bit-rate. Alarms are provided for both Loss Of Lock (LOL) and Loss Of Signal (LOS), and a CDR bypass feature allows direct connection of the input data to the output buffer without re-timing. The CX20501 I/O pin configuration is a drop-in replacement for the OC-48 CX20464 single-rate quad CDR and complements all of Mindspeed's crosspoint switches. Figure 1 illustrates the quad CDR IC functional block diagram and Table 1 through Table 9 list the CX20501 electrical specifications.

Ordering Information

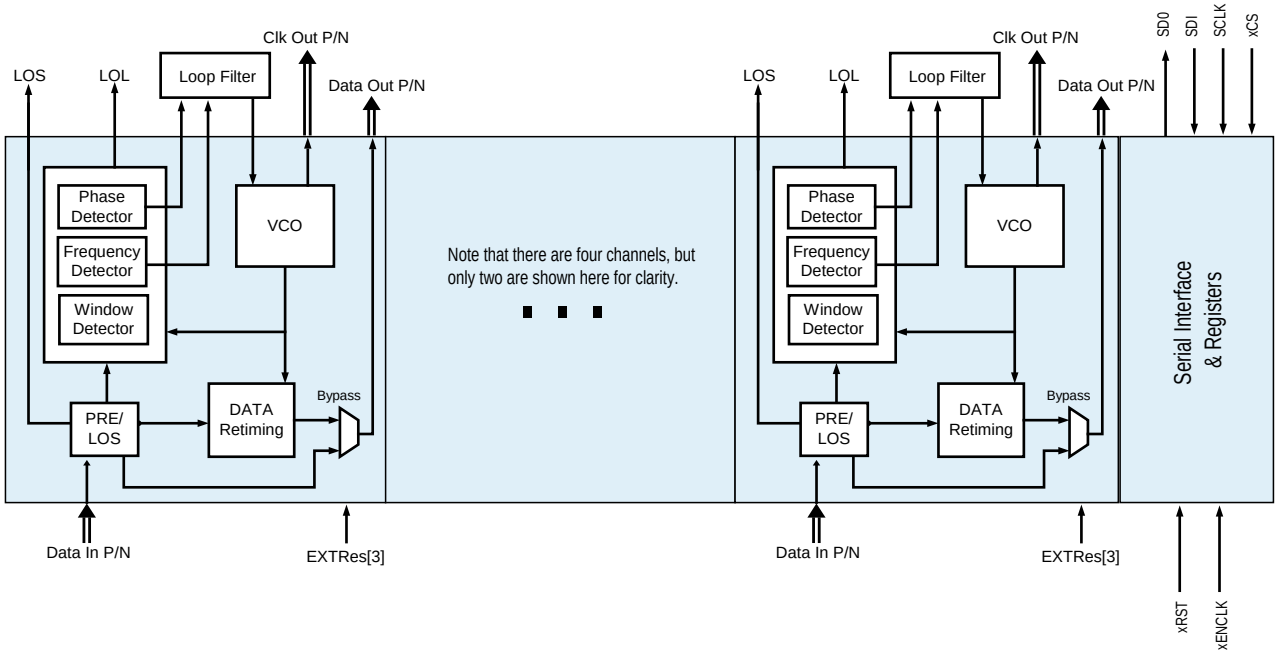
Name	Number	Package Data
CX20501 Quad Multi-rate CDR	CX20501-12	15 mm BGA (196 pin)

Revision History

Revision	Date	Comments
Rev. C	4/02	Converted document to new format. Expanded introduction section. Loop Filter description rewritten. LOS description rewritten. Figures 6 and 7 were added. Tables 1, 2, 3, 4, 6, 7, 8, 9, 10, 17, 18, and 19 were updated.
Rev. D	6/02	Figure 1 redrawn. Figures 4, 5, 10 and 11 updated. Table 14 added. Tables 1, 3, 4, 5, 6, 7, 9, 10, 12, 13, 20 (Output Buffer Level and VCO Control), 21 and 22 updated.
Rev. E	9/02	Tables 8, 9, 10, 11, 13, 14, 20, and 21 were updated. Inserted new Table 18. Revised Figures 7 and 9. Revised the following sections: CDR Archecture, Input Sensitivity/Input Duty Cycle, VCO Frequency Range, Window Frequency Computation, Loop Filter, Loss-Of-Signal and Loss-Of-Lock Bussing, CDR Bypass, Output Drive Level, Other Features, Timing Diagrams: Clock Set and Program Modes.
Rev. A	12/02	Revised Document Number.
Rev. B	3/03	Updated specifications with electrical characterization results.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Figure 1. Block Diagram



SmartCenter™ patent no. US 6,316,966 B1 granted Nov 13, 2001

Introduction

This document uses the following text styling conventions: CDR signal names and terminal numbers are listed with initial caps denoting each functional name part, with its related signal polarity indicated by an upper case 'N' or 'P'. Thus, data input signal names are indicated, for example as: 'DinP' and 'DinN'.

A signal name and an associated CDR channel number (0 through 3) are indicated as DinP[n] and DinN[n] where 'n' is a channel number. Register names are preceded by the word 'register' and typed in all upper case with each functional name part separated by an underscore. Additionally, brackets group register bit numbers, and sub-function parts are in initial caps such as for example: 'register CONTROL_FUNCTION[5:4] Los_hyst'.

Note: There is no space between the name and the first bracket, and a space after the last bracket. The underscore is unique to hysteresis related register names and not universally used in the CX20501 functional description.

Because this unit has four identical CDRs, unless otherwise noted, the same register name applies to each CDR but different addresses describe an unique register.

To better distinguish terminal names from internal signal names the word terminal is included in all references to input, output, or control terminals, such as for example only: 'terminal LOS controls that function', and 'when the LOS terminal = H this function occurs'. In a similar manner references to signal names include the word signal.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 1. Terminal Functional Description

Name	Function	Notes	Type	Signal
DinP[3:0]	Positive high-speed data input	1	I	PCML
DinN[3:0]	Negative high-speed data input	1	I	PCML
DoutP[3:0]	Positive high-speed data output	—	O	PCML
DoutN[3:0]	Negative high-speed data output	—	O	PCML
CoutP[3:0]	Positive recovered clock output	—	O	PCML
CoutN[3:0]	Negative recovered clock output	—	O	PCML
LOS[3:0]	Loss of signal	5	O	CMOS
LOL[3:0]	Loss of lock	5	O	CMOS
LPPp[3:0]	Positive external loop filter (phase detector)	—	A	Analog
LPPn[3:0]	Negative external loop filter (phase detector)	—	A	Analog
LPPf[3:0]	Positive external loop filter (frequency detector)	2	A	Analog
EXTres[3:0]	External reference resistor (12 KΩ +/- 1% to V_{SS})	—	A	Analog
SClk	Serial I/O clock	—	I	CMOS
xCS	Chip select: active low I/O enable	—	I	CMOS
SDI	Serial data input	—	I	CMOS
SDO	Serial data output (high – Z state when not selected)	—	O	CMOS
xENClk	Global HS output clock enable (active low)	—	I	CMOS
xRST	Reset to default state (active Low)	—	I	CMOS
$AV_{DD}C$	Positive supply for CDR core	3	P	PWR
$AV_{DD}O$	Positive supply for output drivers	3	P	PWR
$AV_{DD}V[3:0]$	Positive supply for VCO	3	P	PWR
$AV_{SS}C$	Negative supply for CDR core	3	P	PWR
$AV_{SS}O$	Negative supply for output driver	3	P	PWR
$AV_{SS}V[3:0]$	Negative supply for VCO	3	P	PWR
DV_{DD}	Positive digital supply	3	P	PWR
DV_{SS}	Negative digital supply	3	P	PWR
Ftest[3:0,d:a]	Mindspeed Technologies test pins	4	I	MSPD reserved
Test[3:0,c:a]	Mindspeed Technologies test pins	4	I/O	MSPD reserved

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 1. Terminal Functional Description

Name	Function	Notes	Type	Signal

Notes:
1. Higher input sensitivity and common-mode range over standard PCML.
2. LPPf is a separate pin for lower noise.
3. Separate on-chip power and grounds are maintained for all four CDRs and connected together with a low inductance plane in the package except for the VCO supplies.
4. Leave Mindspeed test pins floating.
5. Various signals from different CDRs can be connected in parallel to form a LOS/LOL bus if enabled in the OUTBF_CTRL[5:4] register.

Table 2. Power DC Electrical Specifications (1)

Symbol	Item	Notes	Minimum	Typical	Maximum	Units
Diss	DV_{DD}: control logic	2	—	0.23	.75	mA
AissC	$AV_{DD}C$: CDR core/per CDR	—	—	46	48	mA
AissV	$AV_{DD}V$: VCO/per CDR	2	—	20	21	mA
AissO	$AV_{DD}O$: output drivers/per CDR	2, 3	—	24	25	mA
I_{total}	Total current/per CDR	2	—	90	93	mA
P_{diss}/CDR	Total power dissipation per CDR	4	—	300	330	mW
P_{diss}	Total quad power dissipation	4, 5	—	1.2	1.32	W

Notes:
1. Specified at Recommended Operating Conditions. See Table 7.
2. Total current computed per CDR channel
3. Computed with clock outputs disabled, data outputs in low output swing mode, and phase lock loop (PLL) in lock
4. Typical P_{diss} computed at +3.3 V and maximum PDISS computed at +3.6 V
5. With both clock and data outputs enabled on all four CDRs in high-swing mode, typically, power dissipation is 1.6W

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 3. +3.3V CMOS DC Electrical Specifications (1,2)

Symbol	Item	Notes	Minimum	Typical	Maximum	Units
V_{OH}	Output logic high I_{OH} = –100 µA	—	3.0	3.2	—	V
V_{OH}	Output logic high I_{OH} = –3 mA	—	2.8	3.0	—	V
V_{OL}	Output logic low I_{OL} = 100 µA	—	—	0.08	0.4	V
V_{OL}	Output logic low I_{OL} = 3 mA	—	—	0.24	0.65	V
V_{OL}	Output logic low I_{OL} = 16 mA	—	—	0.64	0.85	V
I_{OH}	Output current (logic high)	—	–3.0	—	0	mA
I_{OL}	Output current (logic low)	—	0	—	3.0	mA
V_{IH}	Input logic high	—	1.5	—	V_{DD} + 0.3	V
V_{IL}	Input logic low	—	V_{SS} – 0.3	—	1.4	V
I_{IH}	Input current (logic high)	—	–380	—	460	nA
I_{IL}	Input current (logic low)	—	–13	—	0	µA

Note:
1. Specified at Recommended Operating Conditions. See Table 7.
2. CMOS I/Os are TTL compatible when the device is powered with +3.3 V

Table 4. +2.5V CMOS DC Electrical Specifications(1)

Symbol	Item	Notes	Minimum	Typical	Maximum	Units
V_{OH}	Output logic high I_{OH} = –100 µA	—	1.5	2.13	—	V
V_{OH}	Output logic high I_{OH} = –3 mA	—	1.35	1.95	—	V
V_{OL}	Output logic low I_{OL} = 100 µA	—	—	0.4	1.4	V
V_{OL}	Output logic low I_{OL} = 3 mA	—	—	0.54	1.25	V
V_{OL}	Output logic low I_{OL} = 16 mA	—	—	0.78	1.12	V
I_{OH}	Output current (logic high)	—	–3.0	—	0	mA
I_{OL}	Output current (logic low)	—	0	—	3.0	mA
V_{IH}	Input logic high	—	1.1	—	V_{DD} + 0.3	V
V_{IL}	Input logic low	—	V_{SS} – 0.3	—	1.0	V
I_{IH}	Input current (logic high)	—	–380	—	460	nA
I_{IL}	Input current (logic low)	—	–13	—	0	µA

Notes:
1. Specified at Recommended Operating Conditions. See Table 7.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 5. +3.3V PCML DC Electrical Specifications(1)

Parameter	Notes	Minimum	Typical	Maximum	Units
Input differential voltage (peak-to-peak)	2, 4	20	—	1200	mV
Input common-mode voltage	3, 4	V_{DD} – 500	—	V_{DD} + 100	mV
Differential output voltage—high swing (peak-to-peak)	2	730	—	960	mV
Differential output voltage—low swing (peak-to-peak)	2	410	—	560	mV
Low swing: output logic high	5	V_{DD} – 40	—	V_{DD}	mV
Low swing: output logic low	5	V_{DD} – 280	—	V_{DD} – 240	mV
High swing: output logic high	5	V_{DD} – 45	—	V_{DD}	mV
High swing: output logic low	5	V_{DD} – 480	—	V_{DD} – 400	mV

Notes:
1. Specified at Recommended Operating Conditions. See Table 7.
2. Example 1200 mV differential peak-to-peak translates to 600 mV peak-to-peak for each single-ended terminal
3. Designed for DC-coupled PCML or AC-coupled CML, PECL, ECL (ECL may require off-chip attenuation)
4. Absolute maximum differential input voltage and common mode not to exceed V_{DD} +300 mV
5. Output high and output low values are RMS measured values.
6. Clock output swing is typically 60% of data output swing.

Table 6. +2.5V PCML DC Electrical Specifications (1)

Parameter	Notes	Minimum	Typical	Maximum	Units
Input differential voltage (peak-to-peak)	2, 4	20	—	1200	mV
Input common-mode voltage	3, 4	V_{DD} – 500	—	V_{DD} + 100	mV
Differential output voltage—high swing (peak-to-peak)	2	720	—	900	mV
Differential output voltage—low swing (peak-to-peak)	2	380	—	520	mV
Low swing: output logic high	5	V_{DD} – 40	—	V_{DD}	mV
Low swing: output logic low	5	V_{DD} – 260	—	V_{DD} – 225	mV
High swing: output logic high	5	V_{DD} – 45	—	V_{DD}	mV
High swing: output logic low	5	V_{DD} – 450	—	V_{DD} – 380	mV

Notes:
1. Specified at Recommended Operating Conditions. See Table 7.
2. Example 1200 mV differential peak-to-peak translates to 600 mV peak-to-peak for each single-ended terminal.
3. Designed for DC-coupled PCML or AC-coupled CML, PECL, ECL (ECL may require off-chip attenuation).
4. Absolute maximum differential input voltage and common mode not to exceed V_{DD} + 300 mV.
5. Output high and output low values are RMS measured values.
6. Clock output swing is typically 80% of data output swing.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 7. Recommended Operating Conditions

Parameter	Notes	Symbol	Minimum	Typical	Maximum	Units
Core Supply Voltage	1	AvddC	—	2.5/3.3	—	V
Output Supply Voltage	1	AvddO	—	2.5/3.3	—	V
Program Supply Voltage	1	DVddP	—	2.5/3.3	—	V
VCO Supply Voltage	1	AvddV	—	2.5/3.3	—	V
Case Temperature	—	Tc	0	—	+100	°C
Case to ambient thermal resistance	2	θ_{ca}	—	18		°C/W
Case to ambient thermal resistance	3	θ_{ca}	—	23	—	°C/W

Note:
1. Product will operate with +2.5 V ±5% or +3.3 V ±10%
2. θ_{ca} with an airflow velocity of 1 m/sec.
3. θ_{ca} with no airflow, convection cooling only.

Table 8. Absolute Maximum Ratings (1)

Symbol	Item	Minimum	Maximum	Units
DVddP	Program supply voltage	—	3.6	V
AVddC	Core supply voltage	—	3.6	V
AVddO	Output supply voltage	—	3.6	V
AVddV	VCO supply voltage	—	3.6	V
Tst	Storage temperature	–65	+150	°C
ESD	Human body model	1500	—	V
ESD	Charge device model	200	—	V

Note:
1. No Damage.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 9. High-speed PCML or AC-Coupled RF Electrical Specifications (1)

Parameter	Notes	Minimum	Typical	Maximum	Units
Input Bit Rate (NRZ data)	2, 4, 7, 9	2.0/N	—	3.2/N	Gbps
Jitter Transfer	4, 9	—	—	—	Figure
Jitter Tolerance	4, 9	—	—	—	Figure
Jitter Tolerance > 250 kHz	9	0.6	—	—	UI p-p
Clock Jitter Generation (RMS)	3, 4, 6, 10	—	—	0.007	UI rms
Clock Jitter Generation (peak-to-peak)	3, 4, 6, 10	—	—	0.063	UI p-p
Data Output Jitter (RMS)	6, 8, 9	—	7	12	ps
Data Output Jitter (peak-to-peak)	6, 8, 9	—	44	60	ps
Adjacent Channel Isolation	11	30	—	—	dB
Rise Time/ Fall Time (20 to 80%)	6, 11	—	—	100	ps
Output Return Loss (40 MHz to 2.5 GHz)	5, 6, 11	—	–15.0	—	dB
Output Return Loss (2.5 GHz to 5 GHz)	5, 6, 11	—	–5.0	—	dB
Input Return Loss (40 MHz to 2.5 GHz)	5, 6, 9	—	–15.0	—	dB
Input Return Loss (2.5 GHz to 5 GHz)	5, 6, 9	—	–5.0	—	dB

Notes:
1. Specified at Recommended Operating Conditions. See Table 7.
2. Default operation for OC-48 with VCO centered at 2.48832 GHz, device can be programmed to operate at data rates from 2.0/N to 3.2/N Gbps.
3. Measurement jitter bandwidth is 12 kHz to 20 MHz. Clock jitter generation measured per SONET standards.
4. Tested with 50 mV p-p differential input and 2^{23}-1 PRBS pattern.
5. Return loss computed with worst case > 3 sigma 20% variation of resistance
6. Performance specifications listed are for data rates of 2.488 Gbps
7. N = 1, 2, 4, 8, 16, or 32
8. Peak-to-peak jitter increases by approximately 0.06 ps/Mbps at data rates above 2.488 Gbps. RMS jitter increases proportionally.
9. This specification only applies to data.
10. This specification only applies to clock output.
11. This specification applies to both clock and data output.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Figure 2. Jitter Transfer Specification

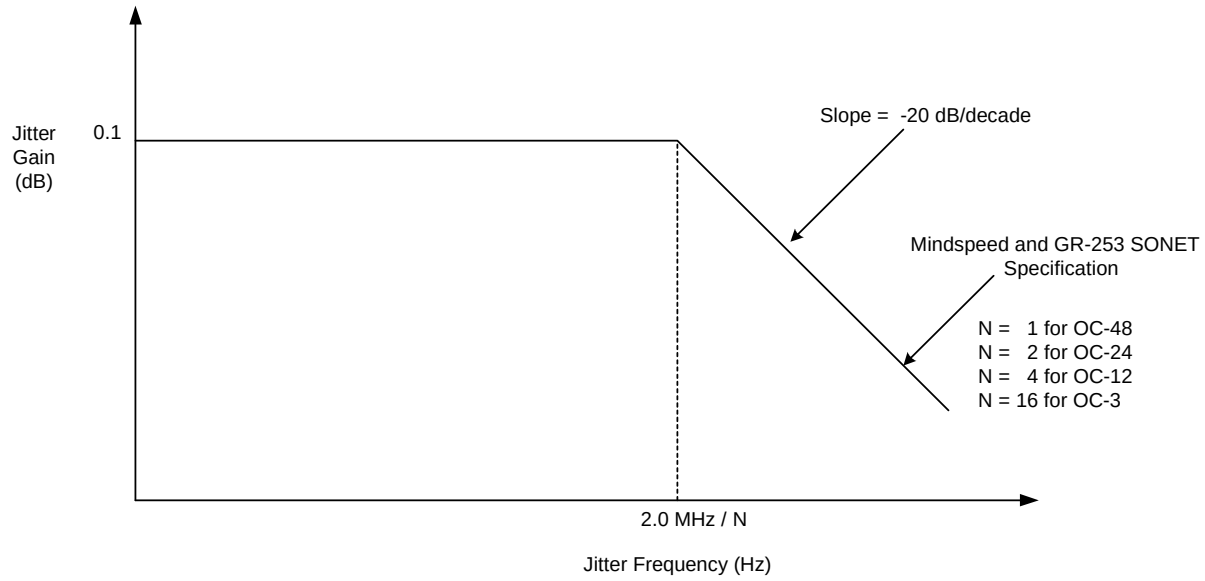
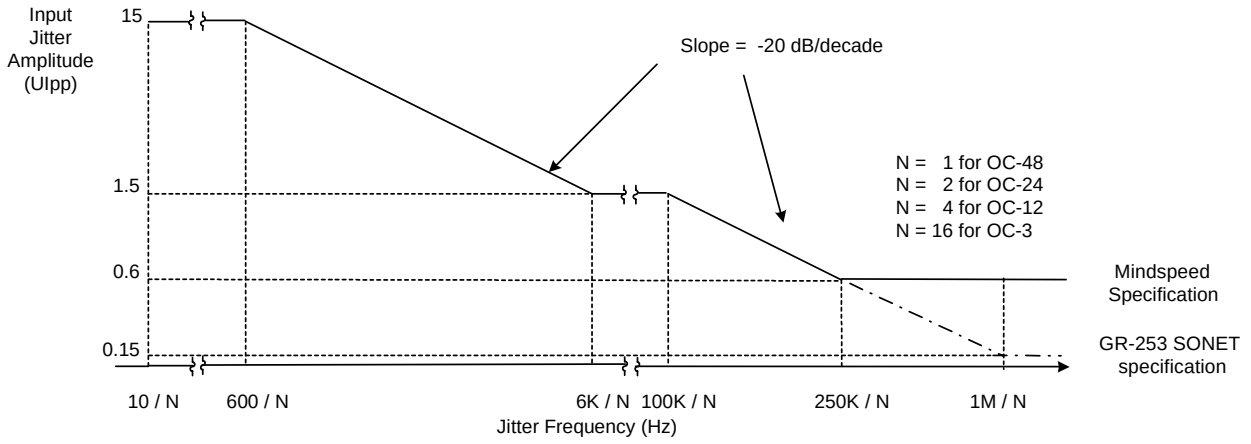


Figure 3. Jitter Tolerance Specification (SONET specification: 0.15 UIpp at 1 MHz)



CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

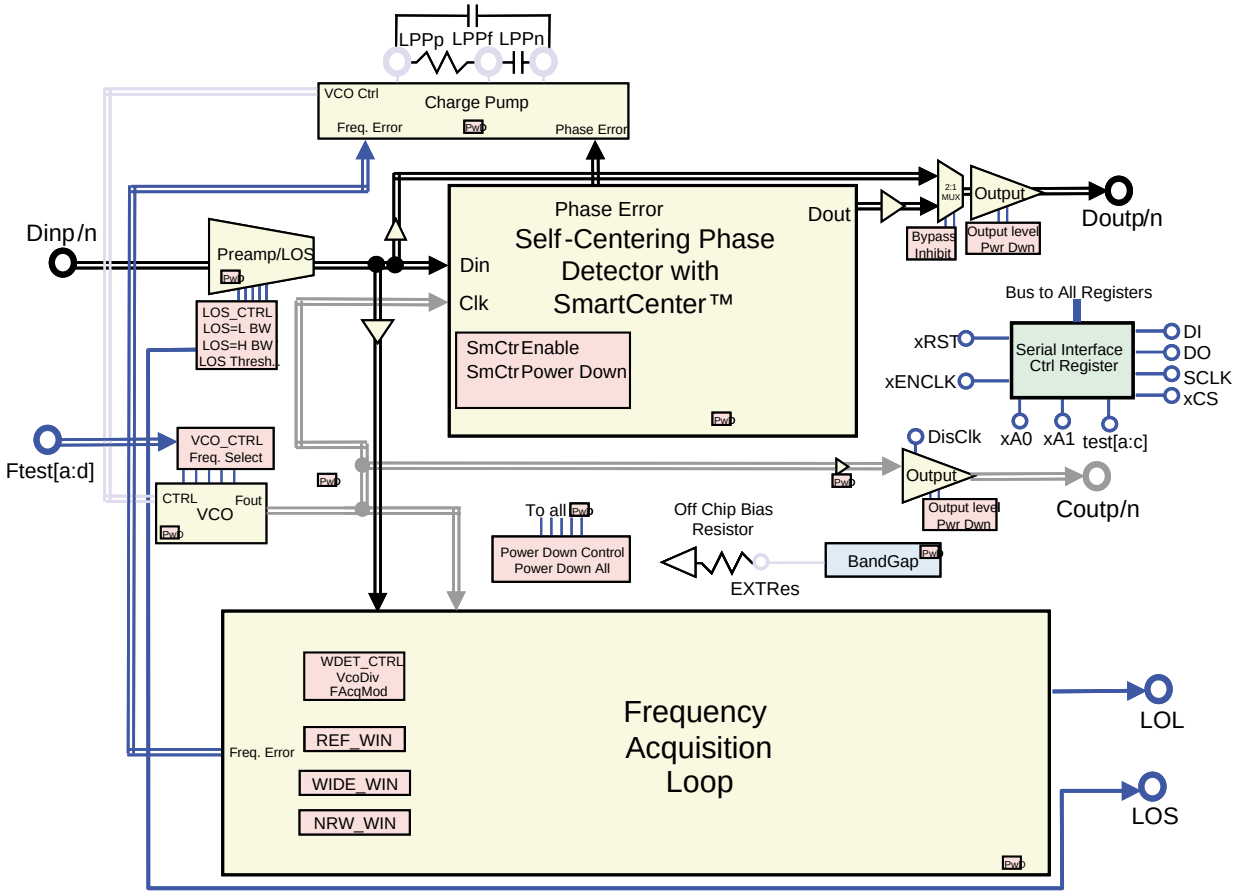
Functional Description

Overview

Figure 4 illustrates the detailed functional block diagram of individual CDRs (the serial interface is not repeated). A serial interface (described in the next section) provides access to the numerous features and options stored in the CX20501 internal memory register.

Table 19 contains a summary of register names, addresses, and bit functions. Table 20 contains a detailed description of the register functions.

Figure 4. CDR Architecture Detail Functional Block Diagram



Reserved and Common Addresses

The following addresses are reserved for various CDRs:

00h-0Dh for CDR#0

40h-4Dh for CDR#1

80h-8Dh for CDR#2

C0h-CDh for CDR#3

Addresses 20h to 25h are common to all four CDRs

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

CDR Architecture

A limiting preamplifier improves input sensitivity and amplifies input data (DinP/DinN) to remove input duty cycle offsets before extracting the recovered clock (CoutP/CoutN) and re-timing the data (DoutP/DoutN).

The input data also passes through a loss-of-signal (LOS) detector to determine if the input signal exceeds a threshold of approximately 240 mV. This design feature, which is based on a self-centering phase detector with a built-in decision circuit, prevents the CDR from locking to noise from a coupled channel. Patented SmartCenter™ topology maintains a centered decision point regardless of data transition density changes (e.g. in the A1/A2 bytes of a SONET header).

SmartCenter™ also keeps the clock centered in the phase margin of the decision flip-flop regardless of temperature, process, and power supply variations. This assures maximum jitter tolerance above the 100 KHz pole.

A frequency detector (FD) works with a frequency window detector (FWD) for frequency acquisition in the absence of an external timing reference. This allows each CDR to operate at different frequencies, which is not achievable with reference based CDRs.

For example, some CDRs can lock to 2.488 Gbps while others may lock at 2.6 or 3.2 Gbps data rates. If the VCO frequency is within the programmable window, the frequency acquisition loop is shut off, so the CDR PLL can achieve phase lock. If not, the frequency acquisition loop is enabled to aid acquisition. The frequency windows differ to increase robustness; the out-of-lock default is: 4,167 ppm and the in-lock default is 93,750 ppm.

IC Partition

All CDRs are identical and each uses a separate on-chip power supply and ground. The individual supplies are connected to low inductance planes within the package; however, each VCO supply is individually brought out for maximum isolation.

Both the positive and negative power supplies are expected to be planes on the printed circuit board (PCB) and all power pins should be bypassed according to standard practices.

The four pairs of supply voltages: $AV_{DD}Vn/AV_{SS}Vn$ (n = 0, 1, 2, 3) should each be bypassed with a large electrolytic capacitor (4.7 µF or larger) along with smaller high-speed capacitors. Unused I/Os and CDRs can be individually powered off to save power and reduce possible sources of crosstalk.

Input Sensitivity/Input Duty Cycle

For improved input sensitivity, input data passes through a preamplifier/quasi-limiting amplifier to amplify the attenuated data signal to full internal logic swing. The differential input sensitivity is 20 mV p-p, which translates to 10 mV p-p on each single-ended input for full logic level into the decision flip-flop. A duty cycle correction servo with a low 3 dB cutoff point of 8 kHz corrects for possible input duty cycle distortion. When enabled, the servo removes any input offset to attain a 50% duty cycle output to the internal decision circuit. To enable this feature, set PD_CTRL0[7] = 0 (default is disabled).

VCO Frequency Range

The default VCO frequency is centered at 2.488 GHz for OC-48 operation. However, to support FEC and non-SONET applications, the VCO frequency can be moved with the VCO_CTRL[6:4] registers. The frequency range is from 2.0 GHz to approximately 3.2 GHz. Mindspeed Technologies centers the OC-48 default setting; the other ranges are approximate. Table 10 and Table 11 show the center frequencies and applications. Table 12 and Table 13 specify the tuning range of each of the center frequencies, grouped by power supply.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 10. VCO Center Frequency Selection

Divider Ratio	Ctrl5	Ctrl4	Ctrl3	Ctrl2	Ctrl1	Ctrl0	Unit
Divide by 1	3200.0	3000.0	2750.0	2500.0	2250.0	2000.0	MHz
Divide by 2	1600.0	1500.0	1375.0	1250.0	1125.0	1000.0	MHz
Divide by 4	800.0	750.0	687.5	625.0	562.5	500.0	MHz
Divide by 8	400.0	375.0	343.8	312.5	281.3	250.0	MHz
Divide by 16	200.0	187.5	171.9	156.3	140.6	125.0	MHz
Divide by 32	100.0	93.8	85.9	78.1	70.3	62.5	MHz

Table 11. Bit Rates of Potential Applications

Divider Ratio	SONET FEC2	ESCON	HDTV	SONET FEC	GigEtherNet	SONET	D1 Video	FibChan	Sysplex	FDDI	Fast Ether	Unit
Divide by 1	**3200.0**	3200.0	2970.0	**2700.0**	2500.0	**2488.3**	2160.0	2124.0	2048.0	2000.0	2000.0	MHz
Divide by 2	1600.0	1600.0	**1485.0**	1350.0	**1250.0**	1244.2	1080.0	**1062.0**	1024.0	1000.0	1000.0	MHz
Divide by 4	**800.0**	800.0	742.5	675.0	625.0	**622.1**	540.0	**531.0**	512.0	500.0	500.0	MHz
Divide by 8	400.0	400.0	371.3	337.5	312.5	311.0	**270.0**	**266.0**	256.0	250.0	250.0	MHz
Divide by 16	**200.0**	**200.0**	185.6	**168.8**	156.3	**155.5**	135.0	**133.0**	128.0	**125.0**	**125.0**	MHz
Divide by 32	100.0	100.0	92.8	84.4	78.1	77.8	67.5	66.5	**64.0**	62.5	62.5	MHz

Table 12. 2.0 to 3.2 GHz Tuning Range Specification for AV_{DD} = 3.3 V (VCO Center Frequency is Approximate)

VCO Setting (GHz)	AV_{DD} = 3.3 V	
	VCO Min (GHz)	VCO Max (GHz)
2.0	2.04	2.20
2.25	2.22	2.43
2.5	2.48	2.71
2.75	2.65	2.87
3.0	2.98	3.28
3.2	3.19	3.37

Table 13. 2.0 to 3.2 GHz Tuning Range Specification for AV_{DD} = 2.5 V (VCO Center Frequency is Approximate)

VCO Setting (GHz)	AV_{DD} = 2.5 V	
	VCO Min (GHz)	VCO Max (GHz)
2.0	1.96	2.10
2.25	2.12	2.30
2.5	2.37	2.56
2.75	2.52	2.70
3.0	2.87	3.09
3.2	3.09	3.28

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Frequency Acquisition

A frequency detector (FD) circuit is employed to determine the frequency difference between the input data and the VCO frequency. Four registers are used to determine the frequency window detector (FWD) characteristics.

First, register WDET_CTRL[4:1] determines the VCO pre-scale value, denoted as N, then register REF_WIN[7:0] sets the reference frequency window, denoted as $W_{ref.}$ The out-of-lock window is set with register NRW_WIN[7:0] (W_{narrow}) and the in-lock window is set with register WIDE_WIN[7:0] (W_{wide}).

When output terminal LOL = H, the PLL is out-of-lock, and a narrow window is used to bring the VCO close to the locking frequency. When output terminal LOL = L, the PLL is in-lock and a wide window signals an out-of-lock condition.

Window Frequency Computation

The window frequency is computed as:

$$F_{narrow} = \frac{W_{narrow}}{W_{ref}} \times 4 \times \frac{f_{vco}}{N} \quad \text{(Used for terminal LOL= H to L)}$$

$$F_{wide} = \frac{W_{wide}}{W_{ref}} \times 4 \times \frac{f_{vco}}{N} \quad \text{(Used for terminal LOL= L to H)}$$

The defaults are:

N = 1536

W_{narrow} = 08h

W_{wide} = B4h

W_{ref} = 5

This implies a 4,167 ppm narrow window and a 93,750 ppm wide window. For OC-48, this translates into windows of 10.4 MHz and 234.4 MHz, respectively. Large values of the W registers will increase the frequency resolution and may also increase the window sample time, which will affect the acquisition time.

Table 14 contains recommended register settings that provide robust frequency acquisition performance for various bit rates. Note that the window values are different for each of the VCO divider ratios and the values listed are decimal values. These suggested values should be considered for use as initial settings, the optimum values for each application may vary slightly.

Table 14. Example Register Settings for Wide and Narrow Frequency Windows (values are in decimal format)

For VCO Divider Ratio:	1	2	4	8	16	32
Ref window address 00h, 40h, 80h, C0h	20	40	80	80	80	80
Narrow window address 01h, 41h, 81h, C1h	58	58	58	58	58	58
Wide window address 02h, 42h, 82h, C2h	59	59	59	59	59	59
Window detector divide ratio address 03h, 43h, 83h, C3h, bits 4:1	1536	1536	1536	3072	6144	12288

With the signal LOLinternal = 1, the frequency acquisition loop (FAL) is enabled to drive the VCO to the narrow frequency window. When the VCO is within the window, the CDR loop is left to obtain phase lock. With signal LOLinternal = 0, the FAL is not enabled until the VCO frequency is beyond the wide window. The signal LOL internal that controls the FAL can be enabled only with a loss of lock (register WDET_CTRL[0] = 0, default), or either the loss of lock or loss of signal (register WDET_CTRL[0] = 1).

The LOL hysteresis function (register WDET_CTRL[7:6] Lol_hyst, address 03h) programs the number of consecutive identical internal loss of lock decisions that must occur before the loss of lock status is modified. This function is controlled by bits 6 and 7 of register 03h, and the default value is to update loss of lock status after one decision.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Data Phase Lock

When the VCO frequency is within the frequency window, the CDR PLL must acquire and maintain phase lock in relationship to the input data. A linear self-centering phase detector centers the clock within the data. SmartCenter™ circuitry in the phase detector (PD) circuit stabilizes the sampling point for process, temperature, power supply, and transition density. With real data, the pattern transition density can change, especially in the A1/A2 bytes in a SONET header. This can cause pattern- dependent jitter if the related PD phase-transfer curves do not intersect at the static phase operating point.

The primary feature of SmartCenter™ is to minimize this source of jitter. The secondary SmartCenter™ feature ensures the clock/data phase-lock relationship is centered within the phase-margin of the decision flip-flop, and provide maximum jitter tolerance over the SONET specifications.

SmartCenter™ can be disabled with register MAST_CTRL[0] = 0 and powered off with register MAST_CTRL[1] = 1. The SmartCenter™ default is power on and enabled.

Loop Filter

A differential RC loop filter is used for low noise and low jitter operation. The CX20501 includes an integrated resistor and capacitor with programmable values so that the loop filter frequency response can be modified for different data rates. In addition to the integrated loop filter components, some external components are required to implement the complete loop filter. See Figure 5 for an illustration of the loop filter topology showing the integrated components as well as recommended external components. The phase detector charge-pump connects between LPPp and LPPn and the frequency detector charge pump connects between LPPf and LPPn. The recommended external loop filter component configuration is shown in Figure 6. A series capacitor with a value of 100 nF should be placed between LPPf and LPPn, and a shunt capacitor with a value of 20 pF should be placed between LPPp and LPPn. If the programmable loop-filter is not desired, connect an external 150Ω low-noise series resistor between LPPp and LPPf in addition to the recommended external series and shunt capacitors.

By default, the data rate selected through VCO_DIV[2:0] programs the correct values for the integrated loop filter components for different SONET rates. LOOP_FILTER[7] = 1 will bypass this default auto-selection, and LOOP_FILTER[6:3] (damping) and LOOP_FILTER[2:0] (bandwidth) set the effective RC value. With auto-selection disabled, the default condition is LOOP_FILTER[6:3] = 0111b and LOOP_FILTER[2:0] = 000b, the latter disabling (open) the internal resistor. If an internal resistor is not selected by LOOP_FILTER[2:0] = 000b, an external resistor of 150 ohms is needed in addition to the two external capacitors. Table 15 summarizes the manual settings, which are used with non-SONET bit rates. In either the auto or manual loop mode, LOOP_TRIM[2:0] provides a trim register for 60% to 130% trim (default is 60% (000b), 100% (100b) should be set for OC-48 operation). This can be used to optimize the performance, especially for nonstandard bit rates.

See Table 15 when selecting internal capacitor and resistor settings.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Figure 5. Internal RC Loop Filter Fine Tune with Recommended External Capacitors

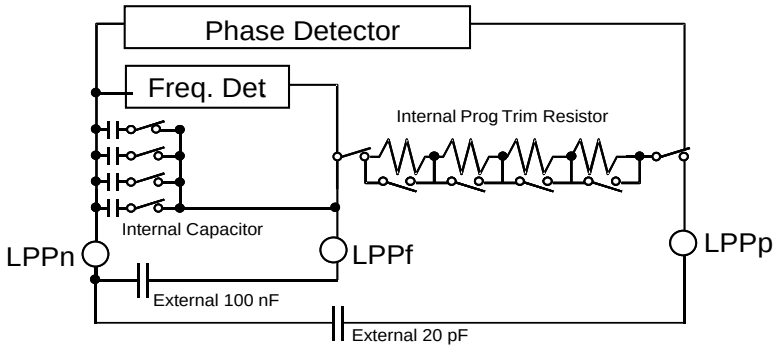


Figure 6. External Loop Filter Configuration

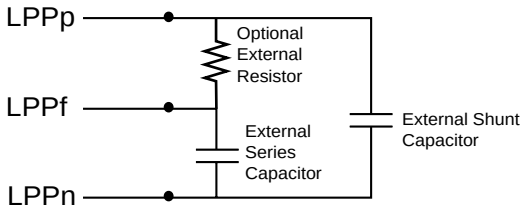


Table 15. Loop Filter Selection

Data Rate (Gbps)	Max. Bandwidth (MHz)	Peaking (dB)	Resistor (Ω)(1)	Damping value(1)
3.1250	2.3	<0.06	150	340
2.7000	2.0	<0.06	150	320
2.4880	1.9	<0.06	150	300
2.0000	1.5	<0.06	150	240
1.2500	0.95	<0.06	300	150
1.0625	0.75	<0.06	300	120
0.622	0.45	<0.06	600	75
0.311	0.23	<0.06	1200	36
0.155	0.10	<0.06	2400	18
0.77	0.055	<0.06	4800	9

Notes:
1. The Resistor and Damping values are programmed in the Loop Filter Adjustment register (0Fh, 4Fh, 8Fh, CFh).

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Loss-Of-Signal

The input data is compared to a threshold in the LOS detector to determine if a signal is present at the input of the CDR or not. There is hysteresis designed into the LOS detector such that the threshold levels are different for a L-H transition and for a H-L transition. The thresholds are set such that LOS will be asserted high if the p-p amplitude of the input signal is below approximately 56 mV.

Once LOS is asserted, the signal will be held high until the p-p input amplitude is greater than approximately 240 mV. If the p-p amplitude of the input signal is greater than 240 mV, then LOS will be held low. If the p-p amplitude of the input signal is between 56 mV and 240 mV, the status of LOS is undefined, and could be high, low, or toggling.

Since the LOS detector looks at the average threshold crossing, the LOS detector has an associated bandwidth. When LOS = L, the default bandwidth of 7.9 KHz (set by LOS_CTRL[7:6]) minimizes false LOS L-to-H transitions with the CDR in-lock.

To quickly enable LOS H-to-L transitions, the LOS = H default bandwidth is 800 KHz (set by LOS_CTRL[5:4]).

Loss-Of-Signal and Loss-Of-Lock Bussing

For applications with one or more CX20501 devices, both the ***LOL*** and ***LOS*** can be wired "OR". In this case, the outputs of ***LOS*** or ***LOL*** will be at a logic high when a loss alarm is active. When the alarm is not active, the outputs will be in a high impedance state instead of logic low. Without any alarms, all outputs are three-stated and requires an external 100 KΩ pull-down resistor connected to ***DVss***. This feature is enabled for Loss-Of-Signal with *OUTBF_CTRL*[5] = 1 (default) and for Loss-Of-Lock with *OUTBF_CTRL*[4] = 1 (default). When either bit is set to 0 and the alarm is not active, the output is pulled low to maintain backward compatibility with the CX20464. When the alarm is enabled, the alarm status of the four CDRs can be read from *LOX_STAT1*[7:0] & *LOX_STAT2*[7:0].

LOX_STAT1/2[7] is ***LOS*** for CDR#3 *LOX_STAT1/2*[3] is ***LOS*** for CDR#1

LOX_STAT1/2[6] is ***LOL*** for CDR#3 *LOX_STAT1/2*[2] is ***LOL*** for CDR#1

LOX_STAT1/2[5] is ***LOS*** for CDR#2 *LOX_STAT1/2*[1] is ***LOS*** for CDR#0

LOX_STAT1/2[4] is ***LOL*** for CDR#2 *LOX_STAT1/2*[0] is ***LOL*** for CDR#0

When the Loss-Of-Signal circuit is powered down, it is forced low when the buss mode is not selected and forced to a high-Z state when the buss mode is selected. *LOX_STAT1*[7:0] always reflects the current status of the alarms. When any individual alarm changes from a no-alarm to an alarm condition, the alarm bit can be immediately read from *LOX_STAT2*[7:0]. The alarm bit stays in the alarm condition until *LOX_STAT2[7:0]* is read, after which the contents of *LOX_STAT1*[7:0] are copied to *LOX_STAT2*[7:0]. If the alarm condition has been resolved, it will clear upon read; if the alarm condition persists, it will remain in an alarm state. A value of '1' in an alarm register indicates the alarm is high (asserted), a value of '0' indicates the alarm is low (not-asserted).

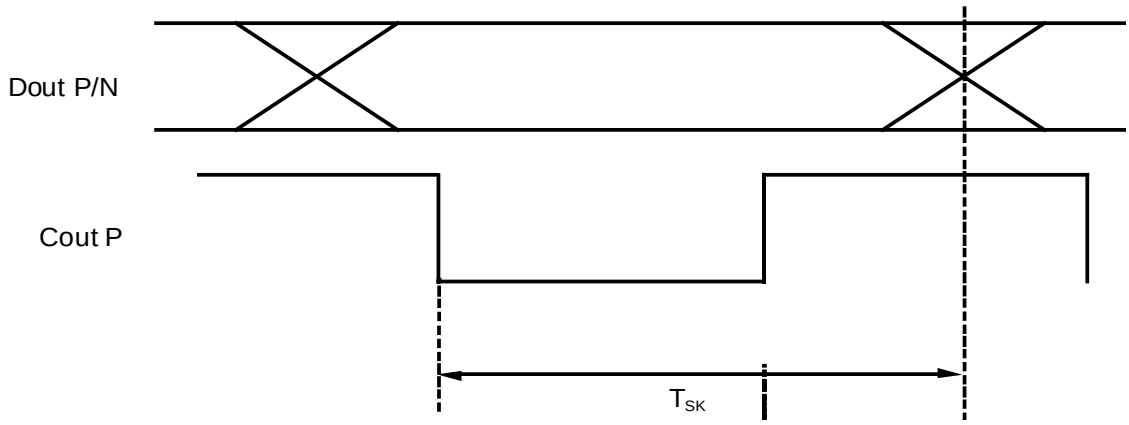
If the ***LOS/LOL*** bussing function is not enabled (*OUTBF_CTRL*[5/4] = 0), the ***LOS*** and ***LOL*** pins and *LOX_STAT1*[7:0] reflect the current status. If the ***LOS/LOL*** bussing function is enabled (*OUTBF_CTRL*[5/4] = 1), *LOX_STAT1*[7:0] always reflects the current status of ***LOS*** and ***LOL***. When bussed, *MAST_CTRL2*[3] = 0 (default) leaves the ***LOS*** and ***LOL*** output pins in a high-Z state. When not bussed, *MAST_CTRL2*[3] = 1 sets the ***LOS*** and ***LOL*** output pins to reflect the current actual status.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Clock to Data Output Timing

The clock and data output skew timing is defined in Figure 7.

Figure 7. Clock and Data Output Skew Timing



The specifications for the clock and data output skew are shown in Table 16, and the specifications for the clock output duty cycle are shown in Table 17.

Table 16. Clock to Data Output Skew

Symbol	Item	Min.	Typ.	Max.	Units
T_{SK}	Skew relative to clock falling edge	245	320	390	ps

Table 17. Clock and Data Output Duty Cycle

Symbol	Item	Min.	Typ.	Max.	Units
C_{DC}	Clock output duty cycle	47	49.4	52.5	%
D_{DC}	Data output duty cycle	44.5	49.4	54.5	%

CDR Bypass

In cases where the input data exceeds the operating range of the CX20501, the CDR re-timing function can be bypassed with *MAST_CTRL2*[4] = 1 (default is with re-timing). Loss-Of-Signal and the Loss-Of-Lock continue to function.

Resetting the CDR

Three different resets are available on the CX20501, one hardware reset and two types of software resets. Any of the three resets loads the default values into the CDR registers of the device. A hardware reset is required after initial power up and is executed by holding the xRST pin low for a minimum of 20 ns, then pulling the xRST pin high. The CX20501 will be available within 20 ns after the xRST pin returns to a high state. In addition to the hardware reset, there are two software resets: A global software reset which resets all four CDRs and an individual software reset that resets a specific CDR channel while leaving the other three CDR channels undisturbed. The global reset is register address 21h and the individual software reset registers are addresses 11h, 51h, 91h, and D1h. To issue either type of software reset, two consecutive writes of AAh to the appropriate address is required. The first write of AAh

puts the device/channel into reset and the second brings the device/channel out of reset.

Output Drive Level

OUTBF_CTRL[3:2] controls the clock drive level and powers the buffer on/off. By default, the register selects power-on, low swing. All four clock outputs are controlled by the ***xENCLK*** pin. If ***xENCLK*** = H, all outputs are off (hardware clock disable has priority over register settings for 500 mV output swing). If ***xENCLK*** = L, the software register, which defaults to low swing for the clock outputs, controls the output drivers. *OUTBF_CTRL*[1:0] selects the output drive level and power the data output driver on/off. The default value is data buffer power-on with low swing.

To minimize noise propagation when several CDRs are chained together, as in a cross-connect application, an inhibit mode is controlled by *MAST_CTRL2*[6:5].

MAST_CTRL2[6:5] = 00b (default) disables the inhibit

01b is a software forced inhibit

10b is inhibit with ***LOL*** = H only

11b is inhibit with ***LOL*** or ***LOS*** = H.

When the inhibit feature is enabled, the output is held H if *MAST_CTRL2*[7] = 1 (default), or L if *MAST_CTRL2*[7] = 0. This feature is automatically disabled if the CDR bypass is enabled. If the output is powered down, the inhibit feature will have no effect until the output driver is powered up. When powered down, the output driver bias is shut-off and both the positive and negative outputs have a 50 Ω pull-up.

Other Features

The *MAST_CTRL*[2] = 1-bit will power-down individual CDR blocks to save power. By default, all four CDRs will power-on after a reset.

NOTE: The serial interface is always on. To minimize noise, SLOPE_CTRL can control the internal / external CMOS bus / serial interface edge rate. For low-speed operation, a slower edge rate reduces the potential of noise generated by the CMOS data edges. For higher speed interface, the edge rate can be increased. This register is global to all CDRs.

For telecom applications, the *CHIP_REV* register contains the current CX20501 revision. This register is global to all CDRs. The *PART_NUMBER* register contains an ID code for this part. Please refer to the latest product bulletin for details on the *CHIP_REV* register contents for the CX20501.

Serial Interface

The CDR functions of the CX20501 are controlled by an 8-bit register. The 8-bit register address and 8-bit data contents are addressed with a serial I/O interface. The different addresses of each register are mapped to a specific function so data can be read from or written to the registers.

Serial I/O Overview

The serial I/O operation is gated by chip select signal xCS (on input terminal xCS). Data is shifted in on terminal SDI on the falling edge of the serial I/O clock input (terminal SCIk), and shifted out on the serial data output (terminal SDO) on the rising edge of SCIk. To address a register, a 10-bit input consists of the first bit (start bit, SB = 1), the second bit (operation bit: OP = 1 for read, OP = 0 for write), followed by the 8-bit address (most significant bit [MSB] first).

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Timing Diagram: Clock Set and Program Modes

The timing diagrams for the serial write and read operations are shown in Figure 8 and Figure 9, respectively. Table 18 contains the specifications for the various timing parameters for the serial programming interface.

To initiate a write sequence, as shown in Figure 8, xCS goes low before the falling edge of SCLK. On each falling edge of SCLK, the 18-bits consisting of the SB = 1, OP = 0, ADDR, and DATA, are latched into the input shift register. The rising edge of xCS must occur before the falling edge of SCLK for the last bit. Upon receipt of the last bit, one additional cycle of SCLK is necessary before the input DATA transfers from the input shift register to the addressed register. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the final read/write cycle to complete the operation.

On a Write cycle, any bits that follow the expected number of bits are ignored, and only the first 16-bits following SB and OP are used.

Figure 9 illustrates the serial Read mode timing diagram. To initiate a read sequence, xCS goes low before the falling edge of SCLK. On each falling edge of SCLK, the 10-bits consisting of SB = 1, OP = 1, and the 8-bit ADDR are written to the serial input shift register of the CX20501. On the first rising edge following the address LSB, the SB and 8-bits of the DATA are shifted out on SDO. The first bit output on SDO for a read operation is always 0.

On a Read cycle, any extra clock cycles will result in the repeat of the data LSB. An invalid SB or OP renders the operation undefined. The falling edge of xCS always resets the serial operation for a new Read or Write cycle. Table 18 contains the timing specifications for the serial programming interface.

Figure 8. Serial Write Mode

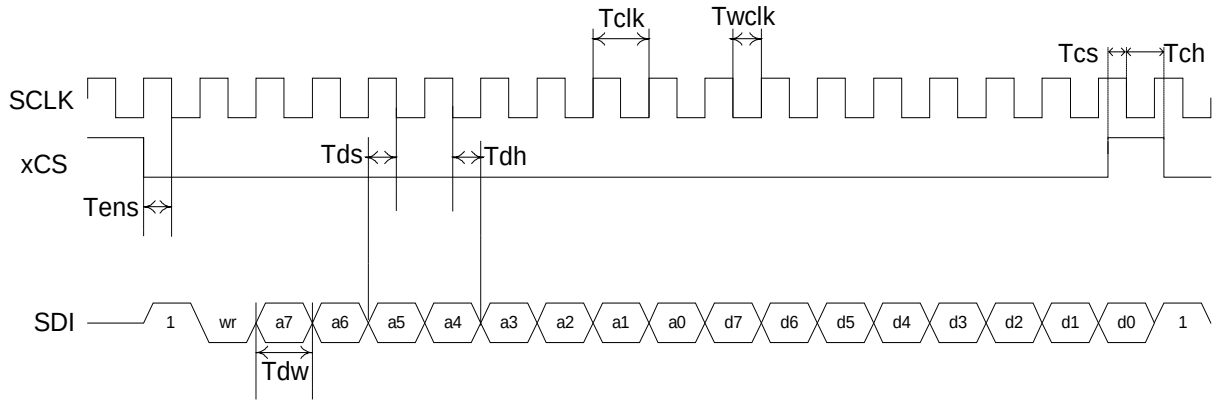
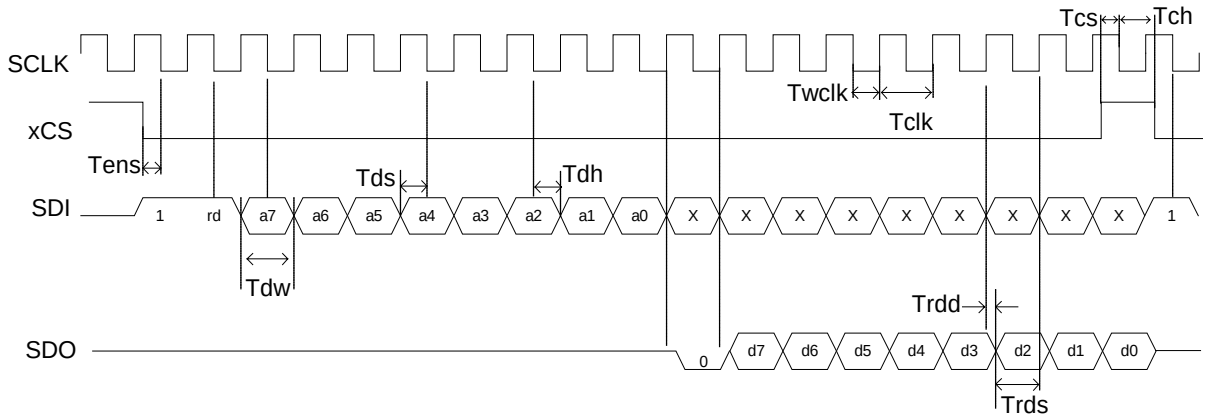


Figure 9. Serial Read Mode



CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 18. Serial Interface Timing—Specified at Recommended Operating Conditions

Symbol	Item	Notes	Minimum	Typical	Maximum	Units
t_{dw}	Data width	—	20	—	—	ns
t_{dh}	Data hold time	—	13	—	—	ns
t_{ds}	Data setup time	—	4.4	—	—	ns
t_{ens}	Enable setup time	—	3.7	—	—	ns
t_{cs}	Chip select setup time	—	3	—	Tclk – 3	ns
t_{ch}	Chip select hold time	—	3.6	—	—	ns
t_{rdd}	Read data output delay	—	8.6	—	23	ns
t_{rds}	Read data valid	—	11	—	—	ns
t_{clk}	SCLK period width	—	20	—	—	ns
t_{wclk}	SCLK minimum low duration	—	5	—	Tclk – 5	ns
t_r	Output rise time	1	—	—	0.66	ns
t_f	Output fall time	1	—	—	0.54	ns

Note:
1. Edge rate in the high edge-rate mode.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 19. Register Summary

Address	Name	d7	d6	d5	d4	d3	d2	d1	d0
00h	REF_WIN	RefWin[7]	RefWin[6]	RefWin[5]	RefWin[4]	RefWin[3]	RefWin[2]	RefWin[2]	RefWin[0]
01h	NRW_WIN	NrwWin[7]	NrwWin[6]	NrwWin[5]	NrwWin[4]	NrwWin[3]	NrwWin[2]	NrwWin[2]	NrwWin[0]
02h	WIDE_WIN	WdWin[7]	WdWin[6]	WdWin[5]	WdWin[4]	WdWin[3]	WdWin[2]	WdWin[2]	WdWin[0]
03h	WDET_CTRL	Lol_hyst[7]	Lol_hyst[6]	“0”	VcoDiv[3]	VcoDiv[2]	VcoDiv[1]	VcoDiv[0]	FacqMod
04h	OUTBF_CTRL			LOSmode	LOLmode	ClkLvl[1]	ClkLvl[0]	DataLvl[1]	DataLvl[0]
05h	LOS_CTRL	LosBiL[1]	LosBiL[0]	LosBoL[1]	LosBoL[0]	“0”	“0”	“1”	“0”
06h	MAST_CTRL			“1”	“1”	“1”	PdAll	PdSmCtr	EnSmCtr
07h	VCO_CTRL	“0”	VcoFreq[2]	VcoFreq[1]	VcoFreq[0]		“1”	“0”	“0”
09h	PD_CTRL0	PdDCservo	“0”	“0”	PdLOS	“0”	“0”	“0”	“0”
0Eh	VCO_DIV						Freqdiv[2]	Freqdiv[1]	Freqdiv[0]
0Fh	LOOP_FILTER	Force	Damp[3]	Damp[2]	Damp[1]	Damp[0]	Bw[2]	Bw[1]	Bw[0]
10h	LOOP_TRIM						Trim[2]	Trim[1]	Trim[0]
11h	ISOFT_RES	“1”	“0”	“1”	“0”	“1”	“0”	“1”	“0”
12h	MAST_CTRL2	InhPol	Inhibit[1]	Inhibit[0]	Bypass	ByPFForce			
(...)									
20h	SLOPE_CTRL			Int[1]	Int[0]			Ext[1]	Ext[0]
21h	GSOFT_RES	“1”	“0”	“1”	“0”	“1”	“0”	“1”	“0”
22h	CHIP_REV	rev[7]	rev[6]	rev[5]	rev[4]	rev[3]	rev[2]	rev[1]	rev[0]
23h	PART_NUM	“0”	“0”	“0”	“0”	“0”	“0”	“1”	“0”
26h	LOX_STAT1	LOS3	LOL3	LOS2	LOL2	LOS1	LOL1	LOS0	LOL0
27h	LOX_STAT2	LOS3	LOL3	LOS2	LOL2	LOS1	LOL1	LOS0	LOL0
(...)									
40h	Repeat CDR1								
80h	Repeat CDR2								
C0h	Repeat CDR3								

Notes:
1. Undefined addresses and bits are reserved for Mindspeed’s use only. A 0 should be written to all undefined bits.
2. Block 20h to 25h is common to all four CDRs.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 20. Register Description (Sheet 1 of 7)

00h, 40h, 80h, C0h: Reference Window		
REF_WIN	[7:0] RefWin	Defines reference window (VCO count period) for the frequency detection timing period. Default RefWin[7:0] = 05h = W_{ref}

01h, 41h, 81h, C1h: Narrow Window		
NRW_WIN	[7:0] NrwWin	Defines narrow frequency window used to signal LOLinternal = 1 to 0. Default NrwWin[7:0] = 08h = w_{narrow}

02h, 42h, 82h, C2h: Wide Window		
WIDE_WIN	[7:0] WdWin	Defines wide frequency window used to signal LOLinternal = 0 to 1. Default WdWin[7:0] = B4h = 180d= w_{wide}

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 20. Register Description (Sheet 2 of 7)

<table>
<tr><th colspan="5">03h, 43h, 83h, C3h: Window Detector Control</th></tr>
<tr><td rowspan="5">WDET_CTRL</td><td>[7:6] Lol_hyst</td><td colspan="3">Defines hysteresis for LOL detection:
00 = LOL gets updated after first detection (default)
01 = LOL gets updated after two consecutive equal LOL values
10 = LOL gets updated after three consecutive equal LOL values
11 = LOL gets updated after four consecutive equal LOL values</td></tr>
<tr><td>[5] MSPD reserved</td><td colspan="3">Mindspeed reserved bit, set to 0.</td></tr>
<tr><td rowspan="16">[4:1] VcoDiv</td><td colspan="3">Determines internal VCO divider ratio (N) for Window Detector
The resulting bandwidth is $w_{(wide \mid narrow)} / w_{ref} * 4 * f_{vco} / N$</td></tr>
<tr><td>VcoDiv</td><td>N</td><td>Bandwidth
(f_{vco} = 2.5 GHz, $w_{(wide \mid narrow)} = w_{ref}$)</td></tr>
<tr><td>0000:</td><td>256</td><td>39.1 MHz</td></tr>
<tr><td>0001:</td><td>512</td><td>19.5 MHz</td></tr>
<tr><td>0010:</td><td>768</td><td>13.0 MHz</td></tr>
<tr><td>0011:</td><td>1024</td><td>9.8 MHz</td></tr>
<tr><td>0100:</td><td>1536 (default)</td><td>6.5 MHz</td></tr>
<tr><td>0101:</td><td>2048</td><td>4.9 MHz</td></tr>
<tr><td>0110:</td><td>3072</td><td>3.255 MHz</td></tr>
<tr><td>0111:</td><td>4096</td><td>2.441 MHz</td></tr>
<tr><td>1000:</td><td>6144</td><td>1.628 MHz</td></tr>
<tr><td>1001:</td><td>8192</td><td>1.221 MHz</td></tr>
<tr><td>1010:</td><td>12288</td><td>0.814 MHz</td></tr>
<tr><td>1011:</td><td>16384</td><td>0.610 MHz</td></tr>
<tr><td>1100:</td><td>24576</td><td>0.407 MHz</td></tr>
<tr><td>1101:</td><td>32768</td><td>0.305 MHz</td></tr>
<tr><td>1110:</td><td>49152</td><td>0.203 MHz</td></tr>
<tr><td>[0] FacqMod</td><td colspan="3">0: LOL enables frequency acquisition (default).
1: (LOS and LOL) enables frequency acquisition.</td></tr>
</table>

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 20. Register Description (Sheet 3 of 7)

04h, 44h, 84h, C4h: Output Buffer Level		
OUTBF_CTRL	[5] LOSmode	Sets operation mode for LOS output 1: Bus operation mode (default) [LOS: true = Voh, false = Hi-Z state] 0: Standard operation mode [LOS: true = Voh, false = Vol]
	[4] LOLmode	Sets operation mode for LOL output 1: Bus operation mode (default) [LOL: true = Voh, false = Hi-Z state] 0: Standard operation mode [LOL: true = Voh, false = Vol]
	[3:2] ClkLvl	Sets output level for clock buffer 00: 900 mV p-p differential swing 01: 500 mV p-p differential swing (default) Has no effect if xENCLK = H, hardware priority 10: Reserved 11: Power-down
	[1:0] DataLvl	Sets output level for data buffer 00: 900 mV p-p differential swing 01: 500 mV p-p differential swing (default) 10: Reserved 11: Power-down

05h, 45h, 85h, C5h: LOS Control		
LOS_CTRL	[7:6] LosBiL	Bandwidth of LOS circuit when LOS = 0 00: 800 kHz 01: 133 kHz 10: 8.3 kHz 11: 7.9 kHz (default)
	[5:4] LosBoL	Bandwidth of LOS circuit when LOS = 1 00: 800 kHz (default) 01: 133 kHz 10: 8.3 kHz 11: 7.9 kHz
	[3:0]	Mindspeed reserved, set to 0010.

06h, 46h, 86h, C6h: Master Control		
MAST_CTRL	[7:3] MSPD reserved	Must be set to 00111b.
	[2] PdAll	0: Power-up entire CDR (default) 1: Power-down entire CDR
	[1] PdSmCtr	0: SmartCenter™ powered up (default) 1: SmartCenter™ powered down
	[0] EnSmCtr	0: SmartCenter™ disabled 1: SmartCenter™ enabled (default)

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 20. Register Description (Sheet 4 of 7)

07h, 47h, 87h, C7h: VCO Control		
VCO_CTRL	[7]MSPD reserved	Must be set to 0.
	[6:4] VcoFreq	VCO Center Frequency 000: 2.0 GHz 001: 2.25 GHz 010: 2.5 GHz (default) 011: 2.75 GHz 100: 3.0 GHz 101: 3.2 GHz
	[3:0] MSPD reserved	Must be set to 0100b.
	Note: 1. VCO Center Frequency is approximate.	

09h, 49h, 89h, C9h: Power-down Control		
PD_CTRL0	[7] PdDCServo	0: Power-on duty cycle servo 1: Power-down duty cycle servo (default)
	[4] PdLOS	0: Power-on loss of signal circuit (default) 1: Power-down loss of signal circuit
	MSPD reserved	All other bits must be 0.

0Eh, 4Eh, 8Eh, CEh: VCO Divider Ratio Control		
VCO_DIV	[7:3] MSPD reserved	Must be set to 00000.
	[2:0] Freqdiv	Determines divide ratio for VCO operating Frequency 000: VCO freq/1 001: VCO freq/2 010: VCO freq/4 011: VCO freq/8 100: VCO freq/16 101: VCO freq/32

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 20. Register Description (Sheet 5 of 7)

0Fh, 4Fh, 8Fh, CFh: Loop Filter Adjustment[1]		
LOOP_FILTER	[7] Force	0: Loop filter adjusted automatically with VCO_DIV (default) 1: Bypass with bits [6:0]
	[6:3] Damp	Fine Tunes Damping value 0000: 9 0001: 18 0010: 36 0011: 75 0100: 120 0101: 150 0110: 240 0111: 300 (default) 1000: 320 1001: 340
	[2:0] BW	Fine Tunes bandwidth resistor value 000: no internal resistor (open) (default) 001: 4800Ω 010: 2400Ω 011: 1200Ω 100: 600Ω 101: 300Ω 110: 150Ω

Note:
1. The data rates and loop bandwidths associated with the resistor and damping values are shown in Table 15.

10h, 50h, 90h, D0h: Internal Loop Filter Trim		
LOOP_TRIM	[2:0] Trim	Fine Tune loop filter bandwidth (should be set to 100% for OC-48 operation) 000: 60% (default) 001: 70% 010: 80% 011: 90% 100: 100% 101: 110% 110: 120% 111: 130%

11h, 51h, 91h, D1h: Individual CDR Software Reset		
ISOFT_RES	[7:0] IReset	A Write access with the value AAh will trigger an internal reset for an individual CDR. The reset will be released by a second Write access with the value AAh.

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 20. Register Description (Sheet 6 of 7)

12h, 52h, 92h, D2h: MAST_CTRL2		
MAST_CTRL2	[7] InhPol	Sets the inhibit polarity 0: DoutP = L when inhibit is enabled 1: DoutP = H (default) when inhibit is enabled
	[6:5] Inhibit	Inhibits the data output with polarity selected with *MAST_CTRL2*[7] 00b: Normal operation (default) 01b: Software force inhibit 10b: Inhibit with ***LOL*** = H 11b: Inhibit with ***LOL*** = H or ***LOS*** = H
	[4] Bypass	0: CDR functional (default) 1: CDR bypassed
	[3] ByPFForce	If the buss LOS/LOL option is selected 0: Output pins always high Z & register status is current (default) 1: Both output pin and register status is current (buss mode disabled)

20h: Slope Control		
SLOPE_CTRL	[5:4] Int	Internal Edge Rate 00: High drive 01: Medium drive 10: Small drive (default) 11: do not use
	[1:0] Ext	External Edge Rate 00: High drive 01: Medium drive 10: Small drive (default) 11: do not use

21h: Global Software Reset		
GSOFT_RES	[7:0] GReset	A Write access with the value AAh will trigger an internal reset of all four CDRs. The reset will be released by a second Write access with the value AAh

22h: Chip Revision Code (read-only)		
CHIP_REV	[7:0] Rev	CDR Chip Revision Code: ...

23h: Mindspeed Part ID Code (read-only)		
PART_NUM	[7:0] Part#	00000010b for CX20501

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 20. Register Description (Sheet 7 of 7)

26h: LOS and LOL Status Register#1 - Actual Status (read-only)		
LOX_STAT1	[7] LOS3	LOS register for CDR#3
	[6] LOL3	LOL register for CDR#3
	[5] LOS2	LOS register for CDR#2
	[4] LOL2	LOL register for CDR#2
	[3] LOS1	LOS register for CDR#1
	[2] LOL1	LOL register for CDR#1
	[1] LOS0	LOS register for CDR#0
	[0] LOL0	LOL register for CDR#0

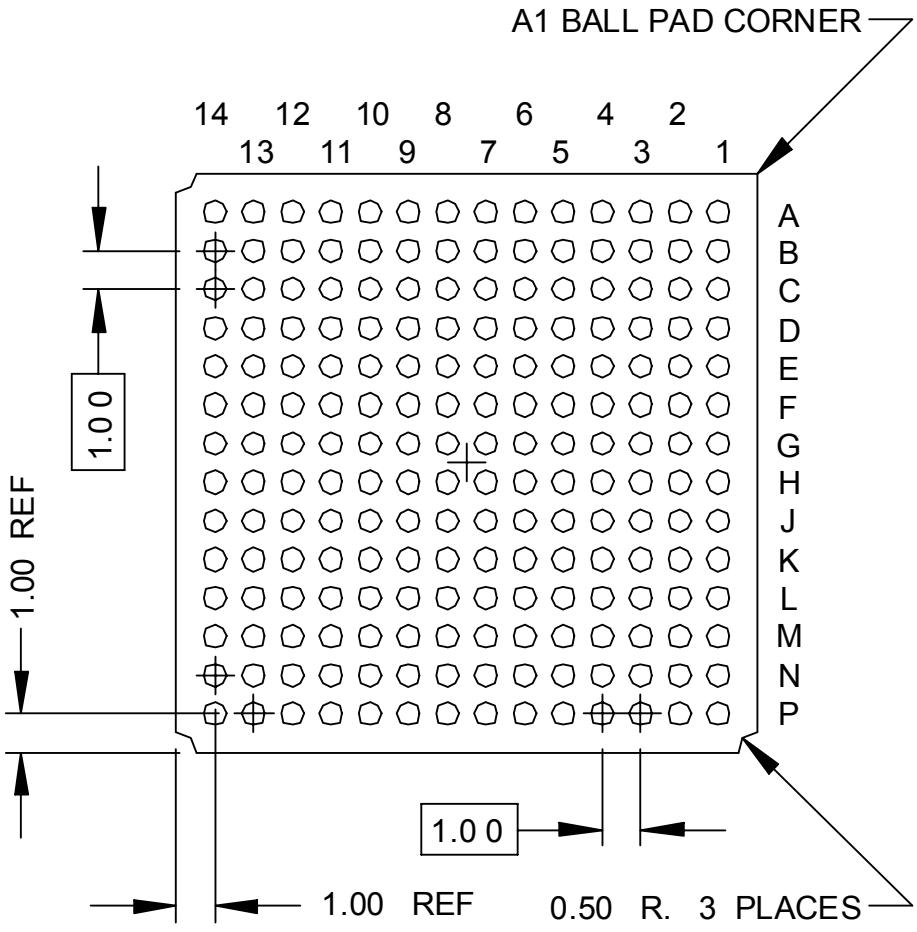
27h: LOS and LOL Status Register#2 - Persistent Status (read-only)		
LOX_STAT2	[7] LOS3	LOS register for CDR#3
	[6] LOL3	LOL register for CDR#3
	[5] LOS2	LOS register for CDR#2
	[4] LOL2	LOL register for CDR#2
	[3] LOS1	LOS register for CDR#1
	[2] LOL1	LOL register for CDR#1
	[1] LOS0	LOS register for CDR#0
	[0] LOL0	LOL register for CDR#0

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Mechanical Specifications

Figure 10 illustrates the ball assignments and package dimensions, Table 21 describes the ball assignment sorted by ball location and Table 22 describes the ball assignment sorted by signal name.

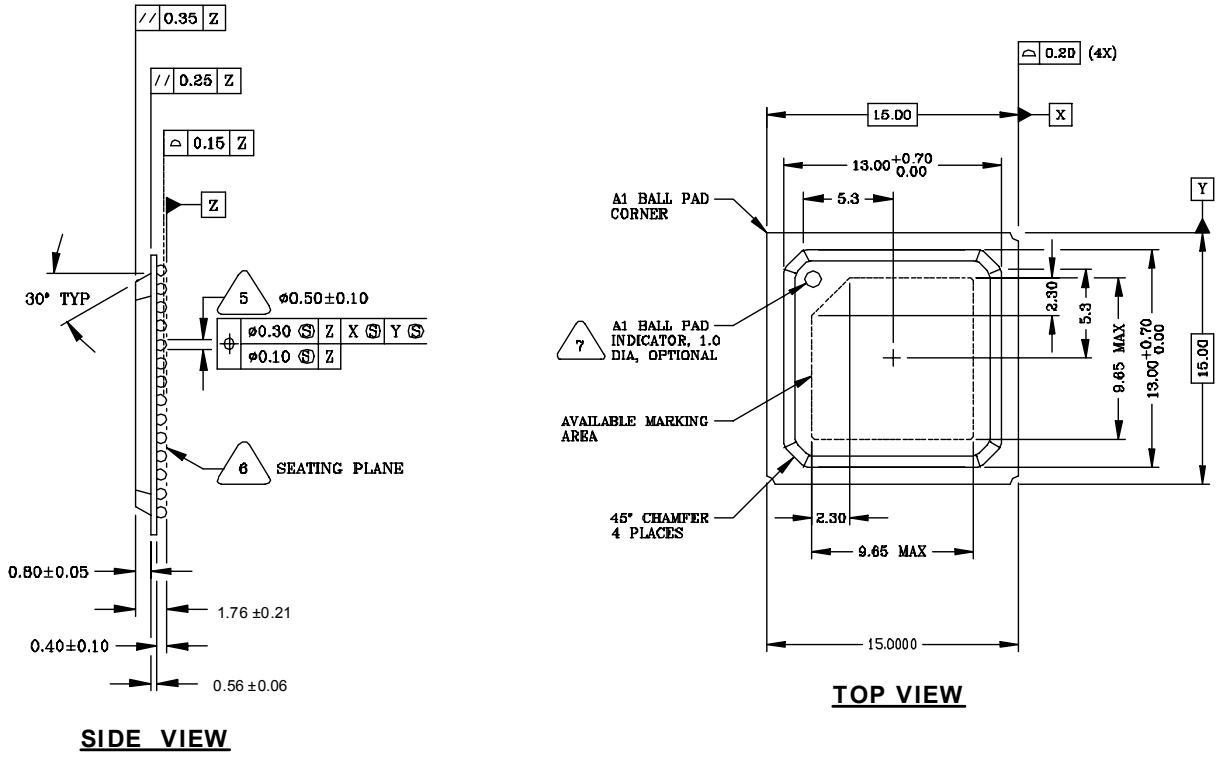
Figure 10. BGA Package Ball Assignment Bottom View (assume package is transparent)



Bottom View 196 Solder Balls
(All dimensions are in mm.)

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Figure 11. Package Drawing



(All dimensions are in mm.)

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 21. Ball Assignment Sorted by Ball Location

Signal	Ball
AvddO	A1
CoutP0	A2
CoutN0	A3
AvssO	A4
DoutP0	A5
DoutN0	A6
AvddO	A7
AvddO	A8
DoutN3	A9
DoutP3	A10
AvssO	A11
CoutN3	A12
CoutP3	A13
AvddO	A14
N/C	B1
AvssV0	B2
AvddO	B3
AvddO	B4
AvddO	B5
AvddO	B6
DVdd	B7
DVss	B8
AvddO	B9
AvddO	B10
AvddO	B11
AvddO	B12
AvssV3	B13
N/C	B14
N/C	C1
AvssC	C2
AvddV0	C3
Ftest0c	C4
AvssO	C5

Signal	Ball
AvssO	C6
DVdd	C7
ExtRes0	C8
ExtRes3	C9
AvssO	C10
Ftest3c	C11
AvddV3	C12
AvssC	C13
N/C	C14
AvssC	D1
AvssC	D2
AvssC	D3
Ftest0a	D4
xRST	D5
xEnClk	D6
xCS	D7
SCLK	D8
SDI	D9
SDO	D10
Ftest3a	D11
AvssC	D12
AvssC	D13
AvssC	D14
DinP0	E1
AvssC	E2
AvssC	E3
Ftest0b	E4
Ftest0d	E5
AvddC	E6
AvddC	E7
AvddC	E8
AvddC	E9
Ftest3d	E10

Signal	Ball
Ftest3b	E11
AvssC	E12
AvssC	E13
DinP3	E14
DinN0	F1
AvssC	F2
LOS0	F3
LPPn0	F4
LPPf0	F5
LPPp0	F6
AvddC	F7
AvddC	F8
LPPp3	F9
LPPf3	F10
LPPn3	F11
LOS3	F12
AvssC	F13
DinN3	F14
Avddc	G1
DVss	G2
LOL0	G3
DVdd	G4
N/C	G5
N/C	G6
N/C	G7
N/C	G8
N/C	G9
N/C	G10
DVdd	G11
LOL3	G12
DVss	G13
AvddC	G14
AVddC	H1

Signal	Ball
DVdd	H2
LOL1	H3
AvddC	H4
AvddC	H5
AvddC	H6
N/C	H7
N/C	H8
AvddC	H9
AvddC	H10
AvddC	H11
LOL2	H12
DVdd	H13
AvddC	H14
DinN1	J1
AvssC	J2
LOS1	J3
AvddC	J4
DVss	J5
N/C	J6
N/C	J7
N/C	J8
N/C	J9
DVss	J10
AvddC	J11
LOS2	J12
AvssC	J13
DinN2	J14
DinP1	K1
AvssC	K2
AvssC	K3
Ftest1c	K4
Ftest1d	K5
LPPn1	K6

Signal	Ball
DVdd	K7
DVdd	K8
LPPn2	K9
Ftest2d	K10
Ftest2c	K11
AvssC	K12
AvssC	K13
DinP2	K14
AvssC	L1
AvssC	L2
AvssC	L3
Ftest1b	L4
LPPp1	L5
LPPf1	L6
AvssO	L7
AvssO	L8
LPPf2	L9
LPPp2	L10
Ftest2b	L11
AvssC	L12
AvssC	L13
AvssC	L14
N/C	M1
AvssC	M2
AvddV1	M3
Ftest1a	M4
AvssO	M5
AvssO	M6
ExtRes1	M7
ExtRes2	M8
AvssO	M9
AvssO	M10
Ftest2a	M11

Signal	Ball
AvddV2	M12
AvssC	M13
N/C	M14
N/C	N1
AvssV1	N2
AvddO	N3
AvddO	N4
AvddO	N5
AvddO	N6
DVdd	N7
DVss	N8
AvddO	N9
AvddO	N10
AvddO	N11
AvddO	N12
AvssV2	N13
N/C	N14
AvddO	P1
CoutP1	P2
CoutN1	P3
AvssO	P4
DoutP1	P5
DoutN1	P6
AvddO	P7
AvddO	P8
DoutN2	P9
DoutP2	P10
AvssO	P11
CoutN2	P12
CoutP2	P13
AvddO	P14

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

Table 22. Ball Assignment Sorted by Signal Name

Signal	Ball
Avddc	G1
AvddC	E6
AvddC	E7
AvddC	E8
AvddC	E9
AvddC	F7
AvddC	F8
AvddC	G14
AvddC	H4
AvddC	H5
AvddC	H6
AvddC	H9
AvddC	H10
AvddC	H11
AvddC	H14
AvddC	J4
AvddC	J11
AVddC	H1
AvddO	A1
AvddO	A7
AvddO	A8
AvddO	A14
AvddO	B3
AvddO	B4
AvddO	B5
AvddO	B6
AvddO	B9
AvddO	B10
AvddO	B11
AvddO	B12
AvddO	N3
AvddO	N4
AvddO	N5

Signal	Ball
AvddO	N6
AvddO	N9
AvddO	N10
AvddO	N11
AvddO	N12
AvddO	P1
AvddO	P7
AvddO	P8
AvddO	P14
AvddV0	C3
AvddV1	M3
AvddV2	M12
AvddV3	C12
AvssC	C2
AvssC	C13
AvssC	D1
AvssC	D2
AvssC	D3
AvssC	D12
AvssC	D13
AvssC	D14
AvssC	E2
AvssC	E3
AvssC	E12
AvssC	E13
AvssC	F2
AvssC	F13
AvssC	J2
AvssC	J13
AvssC	K2
AvssC	K3
AvssC	K12
AvssC	K13

Signal	Ball
AvssC	L1
AvssC	L2
AvssC	L3
AvssC	L12
AvssC	L13
AvssC	L14
AvssC	M2
AvssC	M13
AvssO	A4
AvssO	A11
AvssO	C5
AvssO	C6
AvssO	C10
AvssO	L7
AvssO	L8
AvssO	M5
AvssO	M6
AvssO	M9
AvssO	M10
AvssO	P4
AvssO	P11
AvssV0	B2
AvssV1	N2
AvssV2	N13
AvssV3	B13
CoutN0	A3
CoutN1	P3
CoutN2	P12
CoutN3	A12
CoutP0	A2
CoutP1	P2
CoutP2	P13
CoutP3	A13

Signal	Ball
DinN0	F1
DinN1	J1
DinN2	J14
DinN3	F14
DinP0	E1
DinP1	K1
DinP2	K14
DinP3	E14
DoutN0	A6
DoutN1	P6
DoutN2	P9
DoutN3	A9
DoutP0	A5
DoutP1	P5
DoutP2	P10
DoutP3	A10
DVdd	B7
DVdd	C7
DVdd	G4
DVdd	G11
DVdd	H2
DVdd	H13
DVdd	K7
DVdd	K8
DVdd	N7
DVss	B8
DVss	G2
DVss	G13
DVss	J5
DVss	J10
DVss	N8
ExtRes0	C8
ExtRes1	M7

Signal	Ball
ExtRes2	M8
ExtRes3	C9
Ftest0a	D4
Ftest0b	E4
Ftest0c	C4
Ftest0d	E5
Ftest1a	M4
Ftest1b	L4
Ftest1c	K4
Ftest1d	K5
Ftest2a	M11
Ftest2b	L11
Ftest2c	K11
Ftest2d	K10
Ftest3a	D11
Ftest3b	E11
Ftest3c	C11
Ftest3d	E10
LOL0	G3
LOL1	H3
LOL2	H12
LOL3	G12
LOS0	F3
LOS1	J3
LOS2	J12
LOS3	F12
LPPf0	F5
LPPf1	L6
LPPf2	L9
LPPf3	F10
LPPn0	F4
LPPn1	K6
LPPn2	K9

Signal	Ball
LPPn3	F11
LPPp0	F6
LPPp1	L5
LPPp2	L10
LPPp3	F9
N/C	C1
N/C	M1
N/C	M14
N/C	C14
N/C	B1
N/C	N1
N/C	N14
N/C	B14
N/C	G7
N/C	G6
N/C	G5
N/C	H7
N/C	J7
N/C	J6
N/C	H8
N/C	J8
N/C	J9
N/C	G8
N/C	G9
N/C	G10
SCLK	D8
SDI	D9
SDO	D10
xCS	D7
xEnClk	D6
xRST	D5

CX20501 Quad Multi-Rate CDR (65 Mbps - 3.2 Gbps)

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